SEMICONDUCTOR STORAGE DEVICE AND REFRESH METHOD FOR THE SAME

FIELD OF THE INVENTION

[0001] The present invention relates to a semiconductor storage device and a method of refreshing the semiconductor storage device. More particularly, the present invention relates to a DRAM (dynamic random access memory) capable of inserting a refresh operation during ordinary access operation and an improvement in the method of refreshing the DRAM.

BACKGROUND OF THE INVENTION

[0002] Recently, in low-power-consumption use the replacement of SRAMs (static random accesses memory) with DRAMs has become prevalent for the reason that the memory capacity per unit area of DRAMs is much larger than that of SRAMs. However, DRAM memory cells require the data stored to be refreshed, which is not necessary for SRAMs. Therefore there is a demand for enabling DRAMs to be used by the same method as that for SRAMs in such a manner that automatic refresh using an internal circuit in DRAMs is performed instead of refresh using an external circuit such as a refresh controller.

[0003] Japanese Patent Laid-Open Publication No. 2002-298574 incorporated herein by reference discloses a DRAM using a system in which ordinary read or write operation (hereinafter referred to as "ordinary access operation" or simply as "access operation") and a refresh operation are inserted in a cycle time (hereinafter referred to as "external cycle time"). In this system, since a time period for access and a time period for refresh are secured in an external cycle time, refresh can be performed anytime without postponing ordinary access. A time period for access and a time period for refresh are substantially equal to each other and, therefore, they will hereinafter be referred to collectively as "internal cycle time".

[0004] The external cycle time for this DRAM is actual cycle time, which determines the operating speed. To increase the operating speed of this DRAM, therefore, it is necessary

to reduce the external cycle time. To achieve a reduction in external cycle time, it is necessary to reduce the internal cycle time to a length of time equal to or smaller than half the external cycle time. It is difficult to reduce the external cycle time. This DRAM was designed to enable refresh at any time by securing the internal cycle time for refresh in each external cycle time period. Therefore, only half the real ability of this RAM is used and speedup of this DRAM is difficult.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 is a functional block diagram showing the entire configuration of a DRAM which represents an embodiment of the present invention;

[0006] Figure 2 is a functional block diagram showing the configurations of a decoder block and a decoder control circuit shown in Figure 1;

[0007] Figure 3 is a functional block diagram showing the configuration of an address selector and a refresh circuit shown in Figure 2;

[0008] Figure 4 is a timing chart showing the readout and refresh operations of the DRAM shown in Figures 1 to 3;

[0009] Figure 5 is a functional block diagram showing the configuration of a block control circuit shown in Figure 2;

[0010] Figure 6 is a functional block diagram showing the configuration of the address selector shown in Figures 2 and 3;

[0011] Figure 7 is a timing chart showing the operation of the address selector shown in Figure 6;

[0012] Figure 8 is a timing chart showing the burst refresh operation of the DRAM shown in Figures 1 to 3;

[0013] Figure 9 is a timing chart showing the burst refresh operation as in shown in Figure 8, and particularly showing the operation with respect to various numbers set as N number of ordinary access operations inserted after a refresh operation; and

[0014] Figure 10 is a timing chart showing cases of operation when N = 5, corresponding to the case shown in Figure 9(E): a case (A) where only access operation is performed; a case (B) where refresh and access operations are mixed; and a case (C) where only refresh operation is performed.

SUMMARY OF THE INVENTION

[0015] A main object of the present invention is to provide a semiconductor storage device capable of inserting refresh during ordinary access and capable of speedup and a method for refresh of the storage device.

[0016] A semiconductor storage device in accordance with the present invention has a memory cell array, refresh means, address selection means, word line selection means and selection stop means. The memory cell array includes a plurality of word lines. The refresh means makes a request for refresh and sequentially generates refresh addresses. The address selection means selects access addresses when a request for access is made, and selects the refresh addresses when the request for refresh is made. The word line selection means selects the word lines according to addresses selected by the address selection means. The selection stop means stops address selection performed by the address selection means when the access or the refresh is being performed in the memory cell array.

[0017] A refresh method in accordance with the present invention has a step of making a request for refresh and sequentially generating refresh addresses, an address selection step of selecting an access address when a request for access is made, and selecting from the refresh addresses when the request for refresh is made; a word line selection step of selecting from the word lines according to the selected addresses; and a selection stop step of stopping selection from the access addresses and the refresh addresses when the access or the refresh is being performed in the memory cell array.

[0018] According to the present invention, access addresses are selected when a request for access is made, refresh addresses are selected when a request for refresh is made, and word lines are selected according to the addresses thereby selected. Therefore, a refresh can be inserted during ordinary access. When access or refresh is being performed in the memory cell array, the above-mentioned selection of addresses is stopped. In a case where a request for refresh is made prior to a request for access, therefore, the refresh is performed with priority, and the access subsequently requested is postponed until the refresh started before is completed. Conversely, in a case where a request for access is made prior to a request for refresh, the access is performed with priority, and the refresh subsequently requested is postponed until the access started before is completed. Consequently, the internal cycle time is increased relative to the external cycle time and the external cycle time is thereby reduced to increase the operating speed.

[0019] Preferably, the memory cell array is divided into a plurality of blocks. The above-described semiconductor storage device further has block selection means for selecting from the blocks in response to the address selected by the address selection means. The selection stop means stop the address selection means from performing address selection when the access or the refresh is being performed on the block selected by the block selection means. The above-described refresh method further includes a step of selecting from the blocks in response to the selected address. The selection stop step includes stopping selection from the access addresses and the refresh addresses when the access or the refresh on the selected block is being performed.

[0020] Further, preferably, in the above-described semiconductor storage device, the word line selection means selects all the word lines one after another with respect to each of the blocks in response to the refresh address. In the above-described refresh method, the word line selection step includes selecting all the word lines one after another with respect to each of the blocks in response to the refresh address.

[0021] Since in this case so-called burst refresh is performed on a block-by-block basis, a delay in refresh, if any, can be absorbed during the operation on the selected block and is not carried over to the operation on any of the other blocks.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

[0022] An embodiment of the present invention will be described in detail with reference to the drawings. Identical or corresponding portions are indicated by the same reference symbols and the same description will not be repeated.

[0023] Referring to Figure 1, a DRAM 10 which represents an embodiment of the present invention has a memory cell array 12 including 64M (= 64 x 2^{20}) memory cells MC and 4K (= 4 x 2^{10}) wordlines WL. The memory cell array 12 is divided into 16 access array blocks (hereinafter referred to simply as "blocks") BK. Each block BK includes 256 word lines WL, 16K (= 16 x 2^{10}) bit lines BL intersecting the word lines WL, and 16K sense amplifiers (not shown) connected to the bit lines BL. Each memory cell MC is connected to the corresponding word line WL and bit line BL.

[0024] The DRAM 10 further has a row decoder 14 and a row decoder control circuit 16 which controls the row decoder 14. The row decoder 14 selects from the word lines WL in response to a row address signal. The row decoder 14 is divided into 16 decoder blocks DB, as is the memory cell array 12.

[0025] Figure 2 shows the row decoder control circuit 16 and details of one decoder block DB. Referring to Figure 2, the DRAM 10 further has a refresh circuit 17 and an

address selector 18. The refresh circuit 17 generates a refresh enable signal /RE and sequentially generates a refresh row address signals RRA. The address selector 18 selects an access row address signal ERA externally supplied or the refresh row address signal RRA and supplies the selected signal as a row address signal RA to the row decoder control circuit 16. The row decoder control circuit 16 decodes the supplied row address signal RA to generate row address decoded signals ADU and ADL and supplies these signals to the row decoder 14.

[0026] Figure 3 shows the address selector 18 and details of the refresh circuit 17. Referring to Figure 3, the refresh circuit 17 includes a refresh timer 30, an address counter 32 and a refresh enable circuit 34. The refresh timer 30 generates a refresh timer signal /RT with a predetermined period. The address counter 32 increments the refresh row address in response to the refresh timer signal /RT to generate the refresh row address signal RRA. The refresh enable circuit 34 generates a refresh enable signal /RE in response to a chip enable signal /CE and the refresh timer signal /RT.

[0027] Referring to Figure 4, the chip enable signal /CE is activated to L (logical low) level in each period of external cycle time Tec. Activation of the chip enable signal /CE corresponds to issuing of an access command. When the chip enable signal /CE is activated, the externally supplied access row address signal ERA is taken in the address selector 18 and data is read out from the memory cell MC according to this signal.

[0028] If internal cycle time Tic required for readout or refresh operation is set to one half of the external cycle time Tec, a refresh operation can be inserted with reliability even during readout operation. If the memory cell MC retention time is 64 ms, it is necessary to successively select 4K word lines WL at intervals of 16 μs (= 64 ms / 4K) in order to refresh all the memory cells MC in this time period. Refresh by evenly selecting all the word lines WL one after another with a constant period as described above is called "distributed refresh".

[0029] In the case of distributed refresh, the refresh timer signal /RT is activated to L level with a period of 16 μs independently of the chip enable signal /CE. When the chip enable signal /CE is activated after activation of the refresh timer signal /RT, the refresh enable signal /RE is activated to L level. Activation of the refresh enable signal /RE corresponds to issuing of a refresh command. After a lapse of a predetermined time period after activation of the refresh enable signal /RE, the refresh timer 30 is reset and the refresh timer signal /RT is returned to H (logical high) level. When the refresh enable signal /RE is activated, the refresh row address signal RRA generated by the address counter 32 is taken in the address selector 18 and the memory cells MC are refreshed according to this signal.

[0030] If the internal cycle time Tic is set to one half of the external cycle time Tec as described above, there is no possibility of a refresh command competing with an access command (readout command in this description) and refresh can be performed anytime. In this embodiment, even when a refresh command competes with an access command in a case where the internal cycle time Tic is set longer than half the external cycle time Tec, the competition therebetween is arbitrated to enable insertion of refresh operation during ordinary access operation.

[0031] Referring again to Figure 2, each decoder block DB includes a block enable circuit 20, a row decoder circuit 22, a word line driver 24 and a block control circuit 26. Upper-bit row address decoded signals ADU are supplied to the block enable circuits 20, while lower-bit row address decoded signals ADL are supplied to the row decoder circuits 22. Each block enable circuit 20 generates a block enable signal BE in response to the row address decoded signal ADU to select the corresponding decoder block DB. Each row decoder circuit 22 selects one of the corresponding 256 word lines WL in response to the row address decoded signal ADL. The word line driver 24 drives the selected word line WL. In this embodiment, 12-bit row address signal RA is supplied, a 4-bit signal therein is used for selection from the blocks BK, and the other 8-bit signal is used for selection from the word lines WL.

[0032] The block control circuit 26 is activated in response to the block enable signal BE, receives a timing monitor signal TM from the corresponding block BK, and supplies an array control signal AC to the corresponding block BK. The timing monitor signal TM is generated in the corresponding block BK. The array control signal AC is a signal for controlling activation of the sense amplifier, bit line precharge after restoration, etc., with respect to the corresponding block BK. That is, each block control circuit 26 controls the corresponding block BK so that the sequence of operations is completed in a self-completion manner.

[0033] A feature of this embodiment resides in that the DARM 12 further has one busy signal line 28 for generation of a busy signal BUSY. The busy signal line 28 is provided in common through the 16 blocks BK, and extends in the row decoder 14 parallel to bit line pairs BL.

[0034] Figure 5 shows a circuit for generating the busy signal /BUSY. Referring to Figure 5, each block control circuit 26 includes an array access timing control circuit 36, a delay circuit 38 and an n-channel MOS transistor 40. The array access timing control circuit 36 supplies various array control signals AC including a bit line equalization signal BLEQ to the corresponding block BK. The delay circuit 38 delays the bit line equalization signal BLEQ by a predetermined time period. The transistor 40 is turned on in response to the delayed bit line equalization signal BLEQ to pull down the voltage on the busy signal line 28 to ground voltage GND.

[0035] The row decoder control circuit 16 includes a p-channel MOS transistor 42 and an inverter 44. The transistor 42 is turned on in response to an array enable signal /AE to pull up the voltage on the busy signal line 28 to a power supply voltage VDD. The array enable signal /AE is a pulse signal temporarily generated in response to the chip enable signal /CE or the refresh enable signal /RE.

[0036] When an ordinary access operation or a refresh operation on one of the blocks BK is started, the pulse of the array enable signal /AE is applied to the gate of the transistor

42. The busy line 28 is thereby pulled up to precharge the busy signal BUSY to H level. The busy signal /BUSY is set to L level by the inverter 44 to indicate the one of the blocks BK is operating, thereby prohibiting starting of the next ordinary access operation or refresh operation.

[0037] After the completion of the sequence of operations on the selected block BK, and after a lapse of predetermined time period from the time at which the bit line equalization signal BLEQ is output, the transistor 40 is turned on. The busy line 28 is thereby pulled down to return the busy signal /BUSY to L level. The busy signal /BUSY is returned to H level by the inverter 44 to indicate that the operation on the block BK is completed, thereby canceling the prohibition of the next operation.

[0038] As described above, the busy signal /BUSY is maintained at H level when none of the blocks BK is selected, and it is set to L level when one of the blocks BK is selected. The busy signal /BUSY is maintained at L level until the sequence of operations on the selected block BK is completed. The busy signal /BUSY is supplied from the row decoder control circuit 16 to the address selector 18. That is, the transistor 42 charges the busy signal line 28 according to an access command or a refresh command and discharges the busy signal line 28 when the access operation or refresh operation on the corresponding block BK is completed. The busy signal line 28, the transistor 42 and the 16 transistors 40 provided in correspondence with the 16 blocks BK are means for activating the busy signal /BUSY in response to an access command or a refresh command and deactivating the busy signal /BUSY when the ordinary access operation or refresh operation on the block BK selected by the block enable circuit 20 is completed.

[0039] When the busy signal BUSY is L level, none of the blocks BK is selected and the row decoder control circuit 16 is therefore activated to supply the row address decoded signals ADU and ADL to the row decoder 14. Once one of the blocks BK is selected, the busy signal BUSY is activated to H level, but the row address decoded signals ADU and ADL are maintained in the same state. The row address decoded signals ADU and ADL are not changed regardless of a change in the row address signal RA until the busy signal

BUSY is returned to L level upon completion of the operation on the preceding block BK.

[0040] Figure 6 shows the configuration of the address selector 18. Referring to Figure 6, the address selector 18 includes NAND circuits 46 to 49, inverters 50 and 51, a NOR circuit 52 and a D-type latch circuit 54. N number of NAND circuits 46 to 48 are provided, and N number of D-type latch circuits 54 are provided. In this embodiment, N = 12 since the row address signals ERA, RRA, and RA are 12-bit signals. Twelve NAND circuits 46 input 12-bit access row address signal ERA when the chip enable signal /CE is L level. Twelve NAND circuits 47 input 12-bit refresh row address signal RRA when the refresh enable signal /RE is L level. Twelve NAND circuits 48 output the input 12-bit access row address signal ERA or 12-bit refresh row address signal RRA.

[0041] When the busy signal /BUSY is H level, the NAND circuit 49 functions as an inverter. Therefore, when the chip enable signal /CE or the refresh enable signal /RE becomes L level, a latch signal LT supplied from the NAND circuit 49 to the twelve latch circuits 54 becomes H level. When the latch signal LT becomes H level, the twelve latch circuits 54 take in and latch the 12-bit access row address signal ERA or refresh row address signal RRA output from the twelve NAND circuits 48, and output the latched signal as 12-bit row address signal RA. In short, if the busy signal /BUSY is H level, the address selector 18 selects the access row address signal ERA when the chip enable signal /CE is L level, and selects the refresh row address signal RRA when the refresh enable signal /RE is L level.

[0042] On the other hand, when the busy signal /BUSY is L level, the latch signal LT is fixed at H level. As long as the busy signal /BUSY is L level, even when the chip enable signal /CE or the refresh enable signal /RE becomes L level and when the next new access row address signal ERA or refresh row address signal RRA is input, the latch circuits 54 continue latching the old access row address signal ERA or refresh row address signal RRA and do not take in the next new access row address signal ERA or refresh row address signal RRA. In other words, the operation of the address selector 18

when the busy signal /BUSY is L level is such that even when the chip enable signal /CE or the refresh enable signal /RE becomes L level, the address selector 18 ignores the access row address signal ERA or refresh row address signal RRA subsequently supplied and, instead of selecting this signal, continues outputting the access row address signal ERA or refresh row address signal RRA last selected.

[0043] Referring to Figure 7, when the chip enable signal CE is activated, the access operation on the selected block BK is started and the busy signal /BUSY is activated to L level. When the access operation is completed, the busy signal /BUSY is returned to H level. On the other hand, when the refresh enable signal RE is activated, the refresh operation on the selected block BK is started and the busy signal /BUSY is activated to L level. When the refresh operation is completed, the busy signal /BUSY is returned to H level.

[0044] As described above, the DRAM 10 determines the operation to be subsequently performed according to one of an access command and a refresh command coming ahead of the other when the busy signal /BUSY is returned to H level. Thus, the access row address signal ERA externally supplied and the refresh row address signal RRA internally generated are not discriminated from each other and the operation according to a new row address signal RA is postponed until the operation on the preceding block BK is completed. That is, the DRAM 10 prioritizes the operation according to a command coming ahead of another and postpones the operation according to the subsequent command until the preceding operation is completed.

[0045] In a case where distributed refresh is performed by setting the internal cycle time Tic longer than half the external cycle time Tec, there is a tendency of a refresh command to compete with an access command and refresh is necessarily postponed when such competition occurs. In this embodiment, therefore, it is preferable to perform burst refresh on a block basis in such a manner that burst refresh on each block BK is continuously performed in the shortest time through all the 256 word lines WL.

[0046] To refresh each memory cell MC at intervals of 64 ms, a burst refresh start signal is supplied to each of the 16 blocks BK at intervals of 4 ms (= 64 ms / 16) and burst refresh is continuously performed through the 256 word lines WL in each block BK. In each block BK, therefore, refresh is performed 256 times in the 4 ms period. In actuality, even in a case where the time required for performing refresh one time is 50 ns, the time required for burst refresh is 12. 8 μs (= 256 x 50 ns), extremely short in comparison with 4 ms. Therefore, burst refresh is completed in an initial short time period in the 4 ms period. When an ordinary access command comes during burst refresh, refresh is postponed. In the case of burst refresh on a block basis, however, a delay in refresh is absorbed during the operation on each block BK and is not carried over to any of the other blocks BK, as described below in detail.

[0047] Figure 8 shows a burst refresh operation in a case where access commands A1 and A2 come successively in each period of the minimum external cycle time Tec. A case where the internal cycle time Tic is half the external cycle time Tec, as in the case of the conventional art, is shown in (A), while a case where the internal cycle time Tic is longer than one half of the external cycle time Tec is shown in (B). Description will be made with respect to a case where refresh command R1 comes immediately before an access command A1 and a refresh operation R1 (indicated by the same reference symbol as that for the corresponding command) is thereby started to cause worst conditions in terms of both cycle time and access time for ordinary access operation A1.

[0048] Referring to Figure 8(A), when the refresh command R1 comes immediately before the access command A1, the refresh operation R1 is first started. The refresh operation R1 is completed after a lapse of internal cycle time Tic. Since this refresh is burst refresh, a refresh command is issued each time the preceding ordinary access operation or refresh operation is completed. Therefore another refresh command R2 comes when the refresh operation R1 is completed. At this time, however, the ordinary access operation A1 according to the access command A1 is started since the access command A1 comes at a time T0 before the time at which the refresh command R2 comes. The ordinary access operation A1 is also completed after a lapse of internal cycle

time Tic. This sequence of operations is repeated and refresh operations R1 and R2 in burst refresh and ordinary access operations A1 and A2 are alternately performed. This process will be more concretely below.

[0049] The address selector 18 latches the refresh row address signal RRA in response to the refresh enable signal /RE at L level and supplies the latched refresh address signal RRA to the row decoder control circuit 16. The row decoder control circuit 16 activates the busy signal /BUSY to L level and supplies the row address decoded signals ADU and ADL to the row decoder 14 in response to the refresh row address signal RRA. One block BK is selected in response to the row address decoded signal ADU and one word line WL in the block BK is activated in response to the row address decoded signal ADL to refresh all the memory cells MC connected to the word line WL.

[0050] The chip enable signal /CE is activated to L level during this refresh operation R1 to supply the access row address signal ERA to the address selector 18. However, since the busy signal /BUSY has been activated, the address selector 18 does not latch the access row address signal ERA and continues latching the refresh row address signal RRA last latched.

[0051] When the refresh operation R1 in the selected block BK is completed, the busy signal /BUSY is deactivated to H level. Accordingly, the address selector 18 latches the access row address signal ERA already given, and supplies this signal to the row decoder control circuit 16. Consequently, the ordinary access operation A1 in the selected block BK is performed.

[0052] In the case (A), each ordinary access operation is completed in the external cycle time Tec since the internal cycle time Tic is half the external cycle time Tec. The arrow in the figure indicates the completion of the ordinary access operation from input of the access command. The access time indicated by the arrow is within the external access time Tec, as in the case of SRAMs.

[0053] In the case (B), the internal access time Tic is the same as that in the case (A) but the external cycle time Tec is shorter than that in the case (A). Referring to Figure 8(B), when the refresh command R1 comes immediately before the access command A1, the refresh operation R1 is first performed. Since this refresh is burst refresh, the next refresh command R2 comes immediately after the completion of the refresh operation R1. At this time, however, the ordinary access operation A1 according to the access command A1 is started since the access command A1 comes at time T0 before the time at which the refresh command R2 comes. When the ordinary access operation A1 is completed, another refresh command R3 comes. At this time, however, the ordinary access operation A2 according to the access command A2 is started since the access command A2 comes at time T1 before the time at which the refresh command R3 comes. When the ordinary access operation A2 is completed, another refresh command R4 comes. At this time, the refresh operation R4 according to this refresh command R4 is started since no access command comes before the time at which the refresh command R4 comes.

[0054] In the case (B), the refresh command may be skipped but each memory cell MC is accessed in each period of external cycle time Tec while being refreshed.

[0055] Description will be given with reference to Figure 9 about to which extent the internal cycle time Tic can be extended in a case where the internal cycle time Tic is set longer than one half of the external cycle time Tec.

[0056] The longer the internal cycle time Tic relative to one half of the external cycle time Tec, the less the frequency of insertion of refresh operation. Therefore, a condition for reliably allowing insertion of at least one refresh operation after a certain number of ordinary access operations is required. N number of ordinary access operations are inserted after the internal cycle time (1 x Tic) for the first refresh operation. If the time (N x Tic) required for N number of ordinary access operations is within the N number of periods of the external cycle time (N x Tec), a refresh command comes before the (N +

1)th ordinary access command to start the refresh operation. The condition for insertion of a refresh operation is therefore given by the following expression (1):

[0057] $Tic + N \times Tic < N \times Tec$ ... (1)

[0058] Expression (1) is modified to obtain the following expression (2):

[0059] $Tic < N/(N + 1) \times Tec$ ... (2)

[0060] Expression (2) shows that if the internal cycle time Tic is within the N/(N + 1) multiple of the external cycle time Tec, a refresh operation is inserted before the (N +1)th ordinary access operation. For example, in the case of N = 1, a refresh operation is inserted in every other period if the internal cycle time Tic is shorter than one half of the external cycle time Tec, as shown in Figure 9(A).

[0061] As is apparent from expression (2), the internal cycle time Tic becomes closer to the external cycle time Tec if N is increased. That is, if there is no problem when the frequency of insertion of refresh operations is substantially small, the internal cycle time Tic may be set substantially close to the external cycle time Tec.

[0062] If N is a finite number as shown in Figures 9(A) to 9(E), a refresh command is skipped N times. If N is an infinite number, the internal cycle time Tic is the same as the external cycle time Tec, a refresh command is skipped an infinite number of times, and no refresh operation is inserted, as shown in Figure 9(F). Even if a refresh command comes immediately before the first access command to insert a refresh operation, an access command necessarily comes one cycle before the completion of the preceding access operation and no refresh operation is therefore inserted after the first access operation. If N is not infinite and if the internal cycle time Tic is slightly shorter than the external cycle time Tec, a refresh operation is unfailingly inserted.

[0063] A setting of the upper limit value enabling insertion of refresh operations without exception is then obtained. If the number of word lines per block BK is Nwlb, setting a value obtained by multiplying this number by N x Tec smaller than a value obtained by dividing the retention time Tr by the number of blocks Nb may suffice. The following expression (3) is therefore obtained.

[0064] $N \times Tec \times Nwlb < Tr/Nb$ ... (3)

[0065] Since Nwlb x Nb is the total number Ntwl of word lines, expression (3) is modified by using this to obtain the following expression (4):

[0066] $N < Tr/(Tec \times Ntwl)$ ... (4)

[0067] If the retention time is a typical value of 64 ms; the total number Ntwl of word lines is 4K as in this embodiment; and the external cycle time is 50 ns, the upper limit value of N is a substantially large number about 312.

[0068] If N = 312 is substituted in expression (2), a refresh operation is necessarily inserted at least one time after 312 cycles even when the internal cycle time Tic is 49.85 μs, which is 0.997(= 312/313)/1, i.e., 99.7% of the external cycle time Tec to enable refresh through all the word lines to be unfailingly performed, while ordinary access operations are successively inserted in periods of external cycle time Tec.

[0069] However, even in case where N is not as large as this number, the internal cycle time Tic is substantially close to the external cycle time Tec. For example, the internal cycle time Tic can be increased to 4/5 (= 80%) of the external cycle time Tec when N = 4, that is, refresh operations are inserted in a proportion of one to four ordinary access operations, as shown in Figure 9(D). From the viewpoint of frequency of insertion of refresh operations, even when the external cycle time is 50 ns, the time required for performing burst refresh 256 times is 64 μs (= 5 x 50 ns x 256). In this case, refresh through the 256th word line is delayed most largely. However, the delay of this refresh is

only 51.2 μs (= 64 μs - (50 ns x 256)). This value is only 0.08% of the retention time 64 ms and can be completely ignored.

[0070] Since refresh is performed as burst refresh on a block basis, a delay of refresh can of course be absorbed during the operation on the block BK and is not carried over to any of the other blocks BK and not accumulated. A delay of 51.2 μs is the maximum delay through all the word lines. Thus, according to this embodiment, there is substantially no problem due to refresh delay and the internal cycle time Tic can be increased to become close to the external cycle time Tec. Conversely, a speedup can be achieved by using almost all the real ability of the DRAM 10 capable of operating in the internal cycle time Tic. Thus, an SRAM-compatible DRAM capable of internally performing refresh can be provided and an external cycle time Tec close to one half of that of conventional DRAMs can be achieved.

[0071] Thus, from the viewpoint of "cycle time" it can be said that even when the internal cycle time Tic is longer than one half of the external cycle time Tec, an ordinary access operation and a refresh operation can be performed in the externally cycle period Tec with no problem as long as N is an finite number. However, a problem still exists from the viewpoint of "access time" for ordinary access operation. That is, in ordinary cases of SRAMs, in general the cycle time and the access time are equal to each other. Therefore it is desirable that also in this DRAM 10 data read out should become valid within the external cycle time Tec. However, as shown in Figure 8(B), data first read out (the point of the arrow indicating the access time) is not made valid within the external cycle time Tec, and the access time Tac does not satisfy the ordinary SRAM specification. As is apparent from the figure, to enable the access time Tac to satisfy the specification, it is necessary to set the sum of the internal cycle time Tic for refresh operation and the access time Tac within the external cycle time Tec. In the above-described embodiment, the internal cycle time Tic for refresh operation and the internal cycle time Tic for ordinary access operation are equal to each other. In the case of ordinary access operation, however, the cycle time may be increased in some DRAM as a result of failure to immediately start precharge due to some cause such as page or burst

readout, although the first data access time does not vary. In such a case, it is not necessary to increase the external cycle time Tec and the access time even if the internal cycle time Tic for ordinary access operation is long.

[0072] Also, the access time Tac immediately after refresh operation and the access time Tac after a succession of ordinary access operations differ from each other, as shown in Figure 8(B). Therefore, it is difficult for a user to use the DRAM because of this problem. Then, a method may be used in which, as shown in Figure 10, access latency Tlt is intentionally provided in the specifications to set the sum of the internal cycle time Tic for refresh operation and the internal access time Tic for ordinary access operation as an apparent access time to delay the time at which data becomes valid after a succession of ordinary access operations. The access time Tac is, of course, long, but the cycle time can be shortened. This operation is similar to that in Pipeline Burst SRAM disclosed in Digest of Technical Papers, ISSC91, p.50, Feb. 1991.

[0073] Figure 10 shows cases of operation when N = 5, i.e., a case (A) where only ordinary access commands come, such that the access time Tac is intentionally described as an increased time in terms of specification and is longer than the external cycle time Tec; a case (B) where burst refresh is started when an ordinary access command comes in each period of external cycle time Tec; and a case (C) where only refresh commands come. In the cases (A) and (B), the access times Tac are always the same with respect to input of access commands unlike those shown in Figure 9(E) when N = 5. Even when the access time Tac is longer than the external cycle time Tec, data is successively made valid with the same period as the external cycle time Tec. If data is continuously accessed in this manner, the band width can be increased.

[0074] The present invention has been described with respect to an embodiment thereof. However, the described embodiment is only an example of implementation of the present invention and the present invention is not limited to the described embodiment. The present invention can be implemented by suitably modifying the above-described embodiment without departing from the gist of the invention.

[0075] The semiconductor storage device of the present invention can be used as a DRAM in place of an SRAM particularly in low-power-consumption use.